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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/897,953	07/24/97	KIRA	H 950107A

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EXAMINER	
GRAYBILL,D	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 11/30/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
08/897,953	Kira et al.
Examiner	**Group Art Unit**
David E. Graybill	2814

☒ Responsive to communication(s) filed on *8 Sep 1999*

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *3-6, 8, and 11-17* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *3-6, 8, and 11-17* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☒ The proposed drawing correction, filed on *25 Aug 1999* is ☒ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

Applicant is advised that should claim 3 be found allowable, claim 4 will be objected to under 37 CFR 1.75 as being a duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 11 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Maeda (English translation, JP58180091).

Maeda teaches a process comprising the steps of: (a) forming a plurality of projection electrodes 11 on each of a plurality of semiconductor chips 10; (b) applying a thermosetting insulating adhesive 3 to areas of mounting parts where the chips are to be mounted on a substrate 1; (c) heating the adhesive on the substrate with a half-thermosetting temperature so as to harden the thermosetting insulating adhesive to a half-thermosetting state by heating means 4 and, then, aligning the chips to the mounting parts at a first stage by a bonding head which also holds the chips on the substrate with pressure; (d) moving the substrate to a second stage, while the chips on the mounting part are held at their position by the half-thermosetting state of the adhesive; and (e) thereafter heating, at the second stage, the substrate, on which the chips are fixed, with a

thermosetting temperature of the adhesive, wherein the heating is performed with a pressure applied to the chips are simultaneously heated at the second stage; page 2, lines 19-20; page 3, line 22 to page 4, last line; page 6, antepenultimate paragraph to page 8, line 3; and page 9, first full paragraph.

To further clarify the process comprising a bonding head which also holds the chips on the substrate with pressure, it is noted that this is it is inherent in the process of mounting the chip on the substrate with the bonding head that the head holds the chip on the substrate with pressure.

To further clarify the teaching of a proses comprising wherein the heating is performed with a pressure applied to the chips, Maeda does not teach that the heating is performed in a vacuum; therefore, it is inherent in the process that the heating is performed with an atmospheric pressure applied to the chips.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was

made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 3-6, 8, 11, 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of applicant's admitted prior art and Maeda (English translation, JP58-180091) as applied supra, and further in combination with Koga (JP4302444).

Applicant teaches as conventional a process comprising the steps of forming leveled projection electrode studs 14 on a semiconductor chip 11 by wire-bonding; forming conductive adhesive 16a on the electrodes by a conductive adhesive 16 that has been skidded on a plate 15a and then transcribed onto the electrodes; applying a thermosetting insulating adhesive 18 to areas of mounting parts where the chip is to be mounted on a substrate 17; aligning the chip to the mounting parts at a first stage and performing a first fixing of the chips with a first pressure by a bonding head to which the chip is absorbed; and thereafter, heating the substrate on which the chip is fixed with a thermosetting temperature of the adhesive; page 1, line 23 to page 2, line 22.

However, applicant does not appear to explicitly teach as conventional a process comprising a plurality of chips, and the steps of heating the adhesive on the substrate with a half-thermosetting temperature so as to harden the adhesive on the substrate to a half-thermosetting state by heating means; moving the substrate to a second stage, while the chips on the substrate are held at their position by the half-thermosetting state of the adhesive; thereafter, heating at the second stage the substrate on which the chips are fixed. Nonetheless, Maeda teaches this process at page 2, lines 19-20; page 3, line 22 to page 4, last line; page 6, antepenultimate paragraph to

page 8, line 3; and page 9, first full paragraph. Moreover, it would have been obvious to combine the process of Maeda with the process of applicant's admitted prior art because it would enable accurate alignment of plural chips before the final fixing step of the conventional art.

Further, the combination of applicant's admitted prior art and Maeda does not appear to explicitly teach a process comprising wherein a second fixing is simultaneously performed for each of the chips with a second pressure, and wherein in the heating step (e) while heating the adhesive on the mounting parts a pressure is applied to the chips. Nevertheless, Koga teaches a process comprising wherein a second fixing is simultaneously performed for each of plural chips with a second pressure, and wherein in a heating step while heating an adhesive on mounting parts a pressure is applied to the chips; English abstract and figures. Furthermore, it would have been obvious to combine the process of Koga with the process of the applied prior art because it would facilitate bonding.

Also, the combination of applied prior art does not appear to explicitly teach a process wherein the second pressure is greater than the first pressure. In any case, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed relative pressure limitation is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical, and it appears prima facie that the process would possess utility using another relative pressure. Indeed, it has been held that optimization of range limitations are prima

facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical.

Claims 12 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of applicant's admitted prior art, Maeda and Koga, as applied to claims 3-6, 8, 11, 13 and 15 supra, and further in combination with DiStefano (5548091).

The combination of applicant's admitted prior art, Maeda and Koga does not appear to explicitly teach a process comprising wherein in the heating step (c) heating the adhesive is performed by a heat plate on which the substrate is placed. Regardless, at column 9, lines 3-63 DiStefano teaches a process comprising wherein in a heating step heating the adhesive is performed by a heat plate 58 on which a substrate mounting chips is placed. In addition, it would have been obvious to combine the process of DiStefano with the process of the applied prior art because it would facilitate adhesive curing.

Claims 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of applicant's admitted prior art, Maeda and Koga as applied to claims 3-6, 8, 11, 13 and 15 supra, and further in combination with Fujimoto (5115545).

The combination of applicant's admitted prior art, Maeda and Koga does not appear to explicitly teach a process comprising a heat block having a plurality of pressing/heating heads each of which is provided on the heat block corresponding to the mounting parts of the substrate. Nonetheless, as cited, Koga teaches a process comprising a heat block 25 having a plurality of pressing/heating portions each of which is provided on the heat block corresponding to the

mounting parts of the substrate. Further, at column 6, line Fujimoto teaches a single bonding head 52 for each chip. Moreover, it would have been obvious to combine the process of Fujimoto and the process of Koga by providing the heat block 25 with a single head for each chip because it would enable a pressing force to act evenly on each chip. Furthermore, it would have been obvious to combine the heat block of the combination of Fujimoto and Koga, with the applied prior art because it would facilitate bonding.

Applicant's arguments in the response filed 8-25-99 have been considered but are deemed to be moot in view of the new grounds of rejection.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to the group receptionist at (703) 308-1782.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m..

The fax phone number for group 2800 is (703)305-3431.

David E. Graybill
Primary Examiner
Art Unit 2814

D.G.